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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/620,555	07/17/2003	Bryan D. Boatright	2207/1012902	9247

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EXAMINER	
PEUGH, BRIAN R	

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 08/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/620,555	BOATRIGHT ET AL.	
	Examiner	Art Unit	
	Brian R. Peugh	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *31-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *31,35,36 and 40-42* is/are rejected.

7)☒ Claim(s) *32-34,37-39* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Amendment

This Office Action is in response to applicant's communication filed May 27, 2005 in response to PTO Office Action dated February 23, 2005. The applicant's remarks and amendment to the specification and/or claims were considered with the results that follow.

Claims 31-42 have been presented for examination in this application. In response to the last Office Action, claim 31 has been amended.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 31 and 36 are rejected under 35 U.S.C. 102(b) as being anticipated by Rosen et al. (US# 6,272,595).

Regarding claim 31, Rosen et al. teaches a multiple store buffer forwarding apparatus, comprising: a processor [222] having a write combining buffer [122], and a non-volatile memory coupled to the processor, said non-volatile memory storing instructions which when executed by the processor cause the processor to [although not explicitly recited, processors inherently require non-volatile memories to store all operations to be performed by the processor]: execute a plurality of store instructions

referencing a first memory region [col. 4, lines 55-64; region= cache line]; execute a load instruction referencing a second memory region [col. 4, liens 40-43; col. 5, lines 17-23]; determine that the second memory region matches a cacheline address [col. 5, lines 17-23];determine that the first memory region completely covers the second memory region [write and read addresses match, and therefore 'cover' each other]; transmit a signal to indicate the first memory region completely covers the second memory region [164].

Regarding claim 36, Rosen et al. teaches a multiple store buffer forwarding apparatus, comprising: a memory [12]; a processor [222] coupled to said memory and having write combining buffer [122;], said processor to execute a plurality of store instructions referencing a first memory region [cacheline] of said memory col. 4, lines 40-63]; execute a load instruction referencing a second memory region [cacheline] of said memory [col. 4, lines 40-63]; determine that the second memory region matches a cacheline address [write address=read address]; determine that the first memory region completely covers the second memory region [col. 5, lines 17-23]; and transmit a signal [164] indicating that store buffer forwarding is authorized.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 35 and 40-42 are rejected under U.S.C. 103(a) as being unpatentable over Rosen et al. (US# 6,272,595) and Kumar et al. (US# 6,922,745).

Regarding claim 41, Rosen et al. teaches a processor [222]; a write combining buffer (WCB) [122] coupled to the processor, ...a comparison circuit coupled to the WCB [124], the comparison circuit to receive a load operation from the processor [col. 4, lines 40-48; col. 5, lines 17-23], the comparison circuit to compare a memory region requested by the load operation to addresses of the store data in the WCB [col. 5, lines 17-19], and the comparison circuit to generate a signal [164] indicating that store buffer forwarding is authorized for the load instruction if the memory region [cache line] requested by the load operation can be globally observed in a single atomic transaction [Fig. 4; col. 56, line 52 – col. 6, line 9] and if the store data in the WCB completely covers the memory region requested by the load operation [write and read addresses match, and therefore 'cover' each other].

The difference between the claimed subject matter and that of Rosen et al. is that the claim recites the WCB to combine data from a plurality of processor store operations into a single WCB entry. Kumar et al. teaches WCB to combine data from a plurality of processor store operations into a single WCB entry [col. 4, line 66 – col. 5, line 9].

Therefore it would have been obvious to one of ordinary skill in the art having the teachings of Rosen et al. and Kumar et al. before him at the time the invention was made to modify the write-combine system of Rosen et al. to include the mutli-store combining of Kumar et al., because then many operations could be combined into a

single store operation, thereby reducing the number of memory accesses and improving bus bandwidth.

Regarding claims 35 and 40, Rosen et al. fails to teach that the processor is implemented as a multiprocessor having associated with each said multi-processor a separate set of hardware resources. Rosen et al. teaches that the processor 200] is implemented as a multiprocessor [DAC [263] and SAAT [267]] having associated with each said multi-processor a separate set of hardware resources [[610, 254] & [266], respectively; the units 'process' operations; col. 4, line 66 – col. 5, line 37]. Therefor it would have been obvious to one of ordinary skill in the art having the teachings of Rosen et al. and Kumar et al. to modify the write-combine system of Rosen et al. to include the multi-processing system of Kumar et al., because then a system for detecting incorrect translation and page-walking in order to provide the correct translation, as taught by Kumar et al. [col. 5, lines 20-37].

Regarding claim 42, Rosen et al. teaches wherein each WCB entry is sized to match a system cache line size [cache set address [90].

Allowable Subject Matter

Claims 32-34 and 37-39 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments filed June 5, 2006 have been fully considered but they are not persuasive.

Applicant has argued on pages 7 and 8 that the Rosen et al. reference does not teach to execute a load instruction referencing a second memory region. The Examiner would like to point out that col. 5, lines 17-23 recite the load, or read, operation as claimed. Column 4, lines 40-44 also recite the read operation as claimed. Secondly, in response to Applicant's argument that the data being referenced is from processor 222 and not a memory region, the Examiner is unclear as to where in the Rosen et al. reference this is taught. Lines 42 and 43 of column four are directed towards a read (load) operation from the processor 222 to data stored elsewhere.

The Applicant has argued on page 8 of the response that a match operation is part of a read operation as recited by Rosen et al., and that this read operation does not qualify as a load operation, nor does the read operation reference a second memory region. The Examiner would like to point out that this read operation applies to the load instruction as claimed. Also, Rosen et al. does in fact teach a second memory region. The Examiner has interpreted each cache line as a separate memory region, thus the matching of a set address (90) with a buffered address (162) for a cacheline corresponds to the determination that the first memory region completely covers the second memory region as claimed. Upon this match, or determination, a set compare result (164) causes a buffer to load data.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian R. Peugh whose telephone number is (571) 272-4199. The examiner can normally be reached on Monday-Thursday from 7:00am to 4:30pm. The examiner can also be reached on alternate Friday's from 7:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks, can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brian R. Peugh
Primary Examiner
Art Unit 2187
August 24, 2006